

002250" 2682950

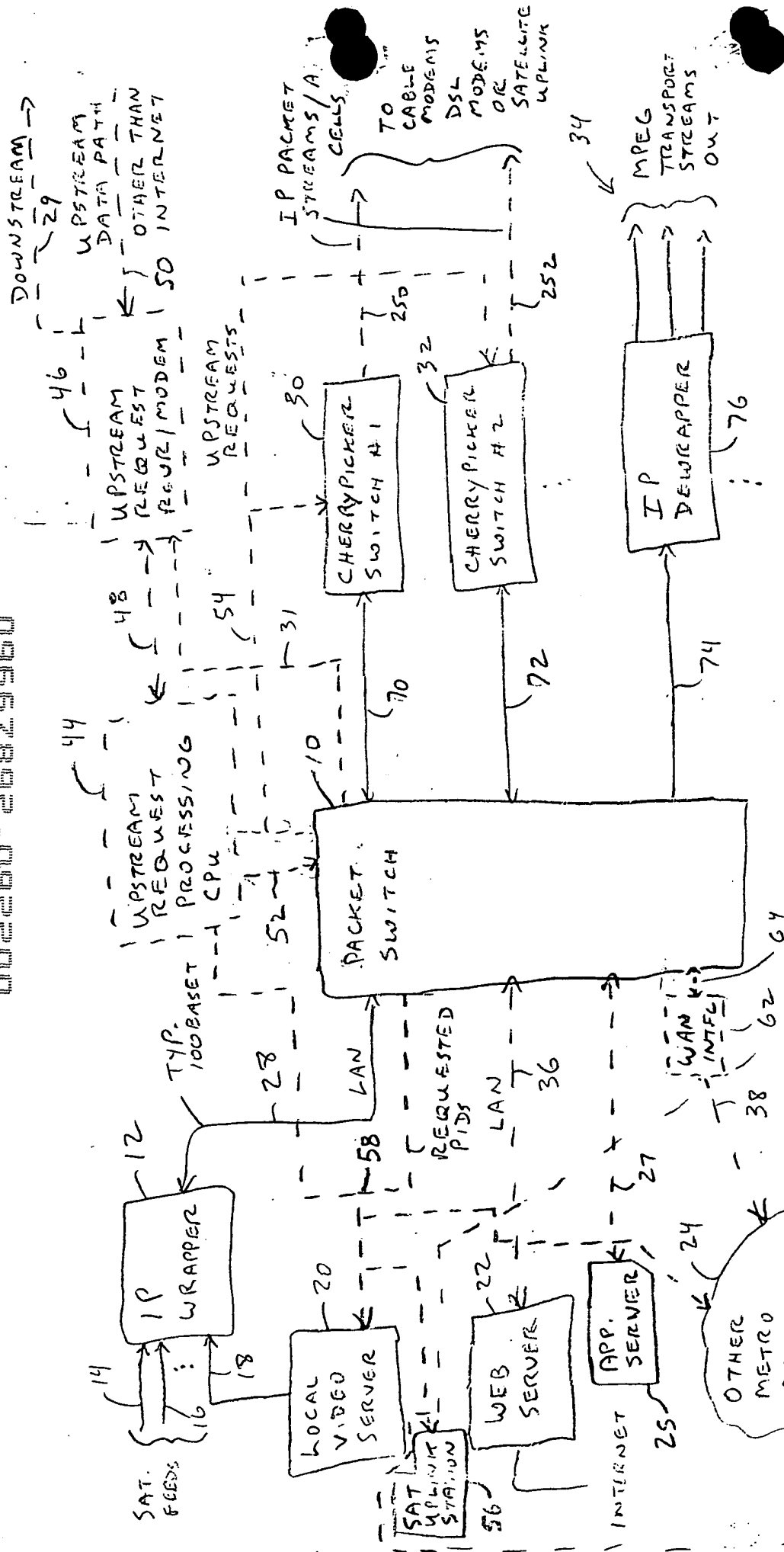
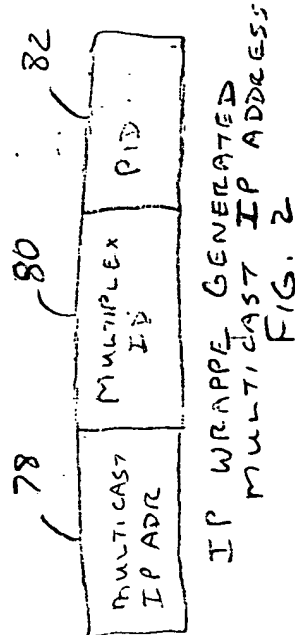


FIG. 1



PROCESS OF ENCAPSULATION CARRIED OUT IN IP WRAPPER FPGA

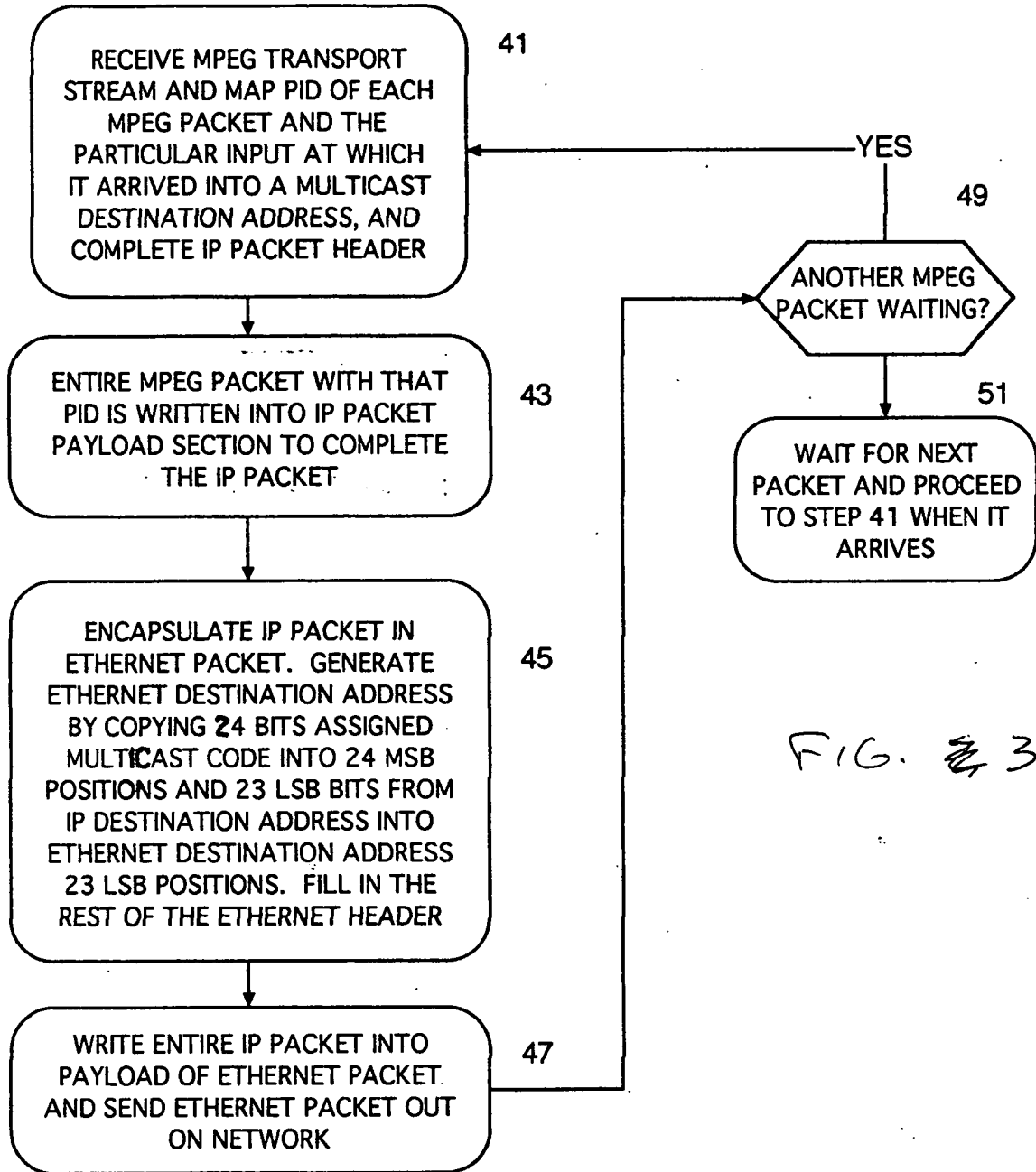


FIG. 3

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PREFERRED ENCAPSULATION PROCESS CARRIED OUT BY IP WRAPPER

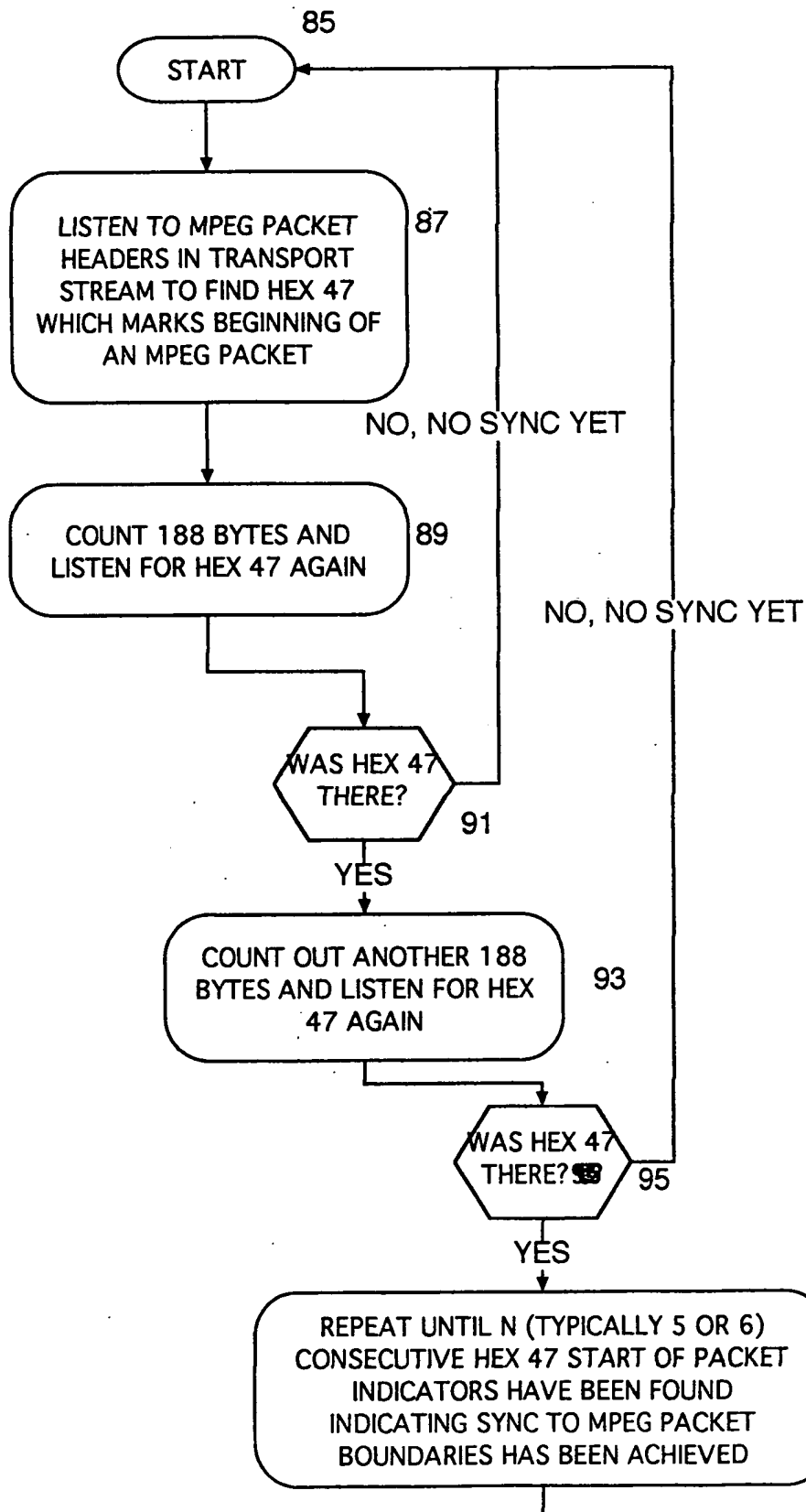
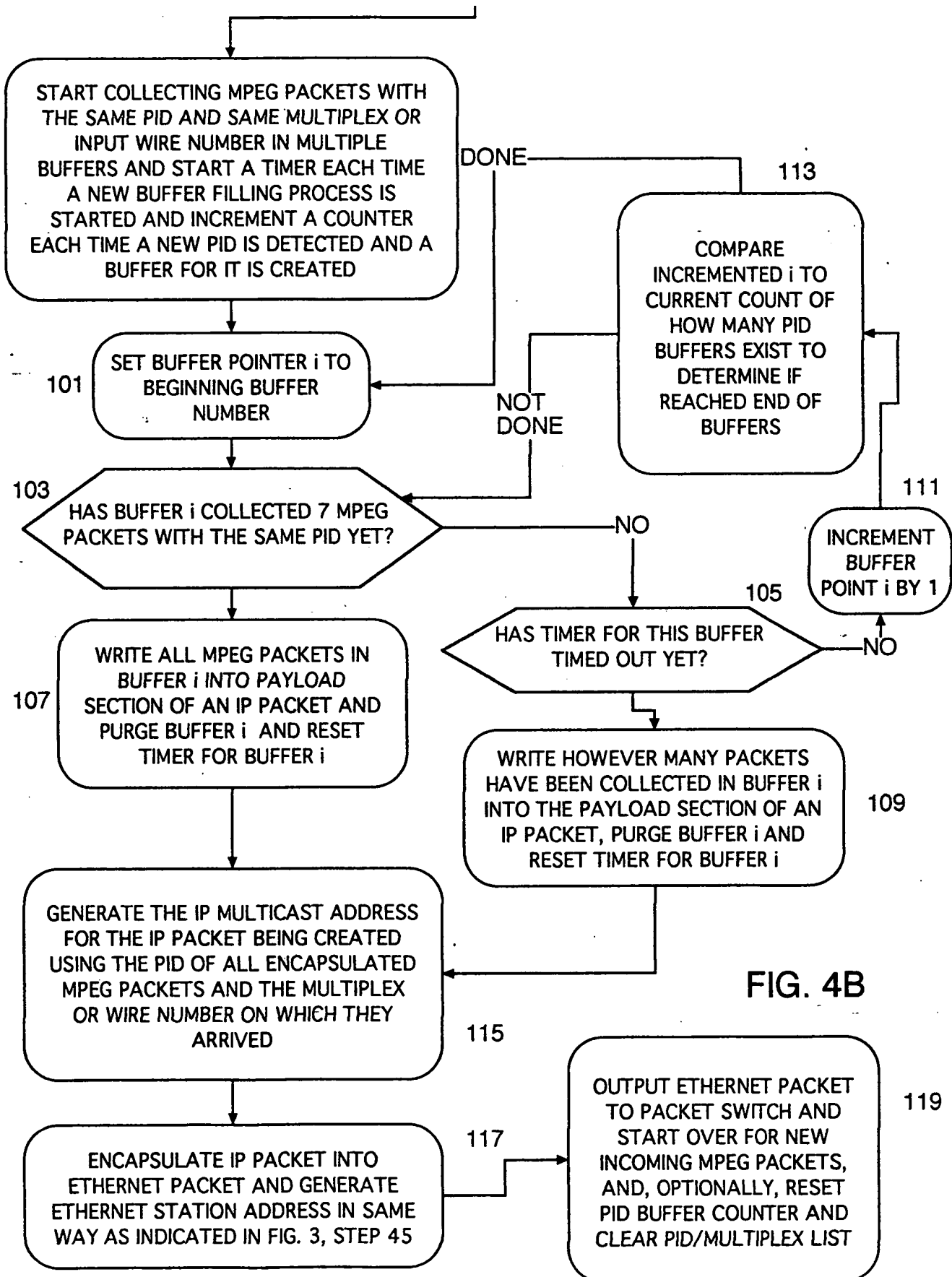


FIG. 4A



PROCESS OF GENERATING MPEG TRANSPORT STREAMS IN CHERRYPICKER SWITCHES

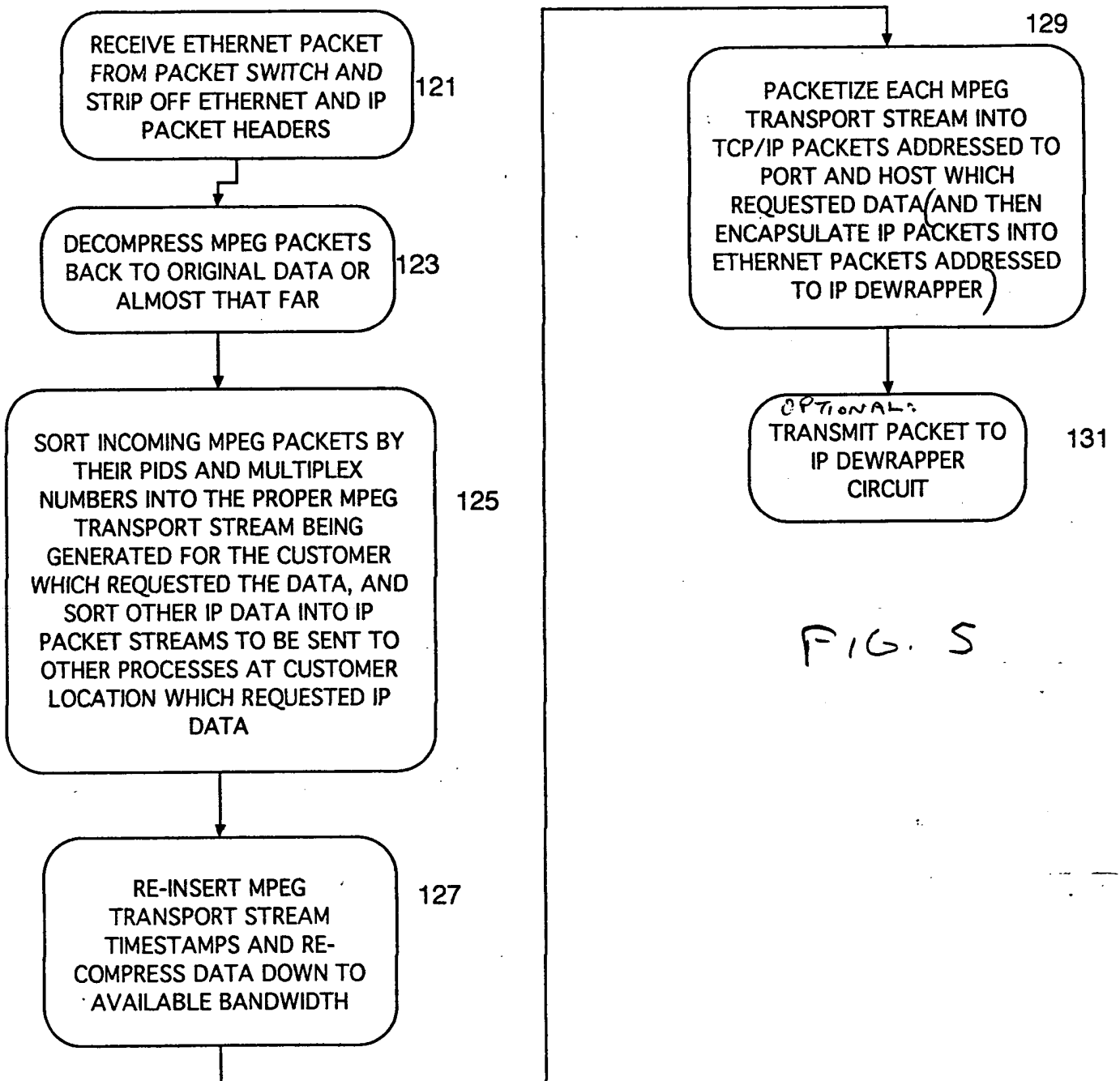
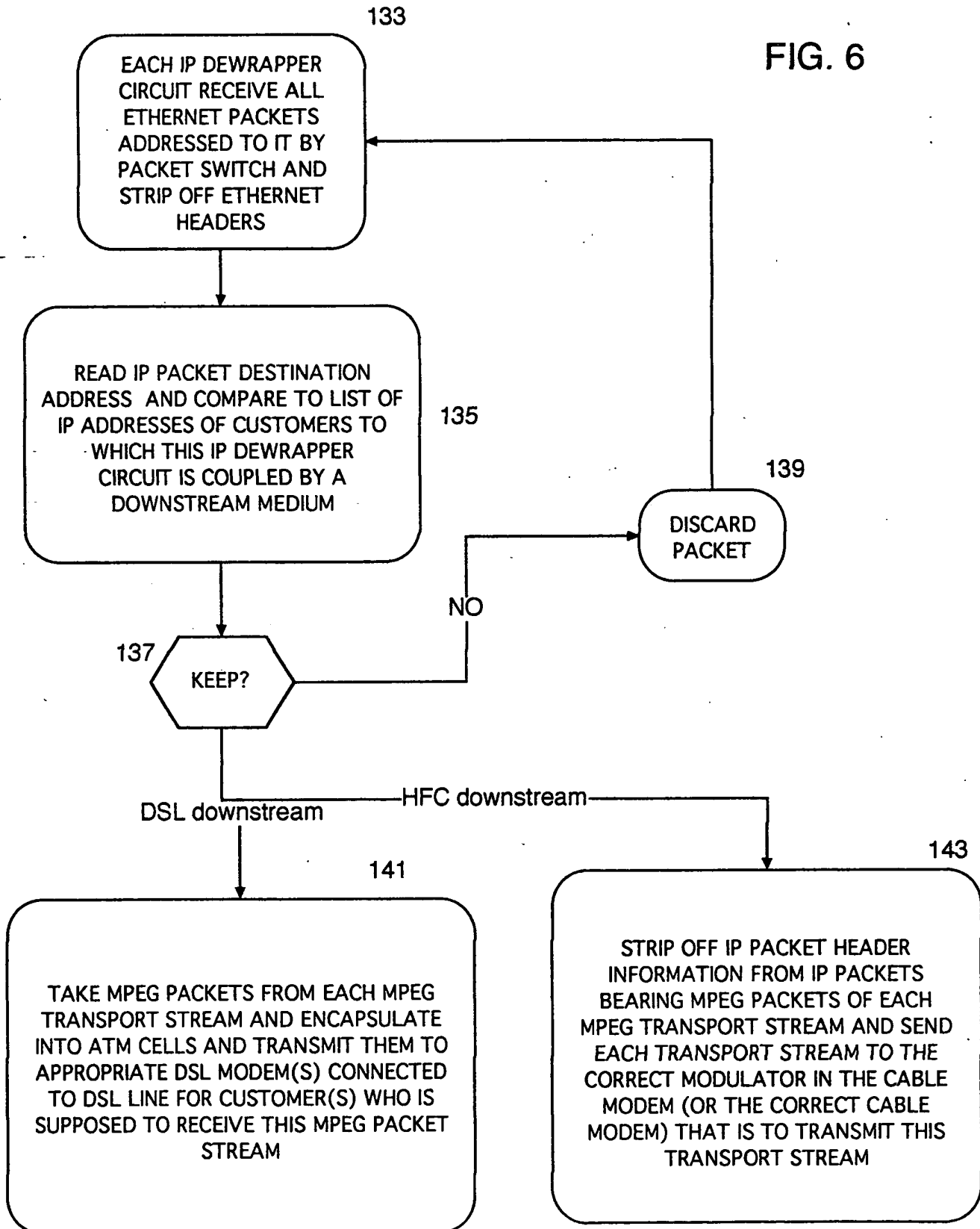
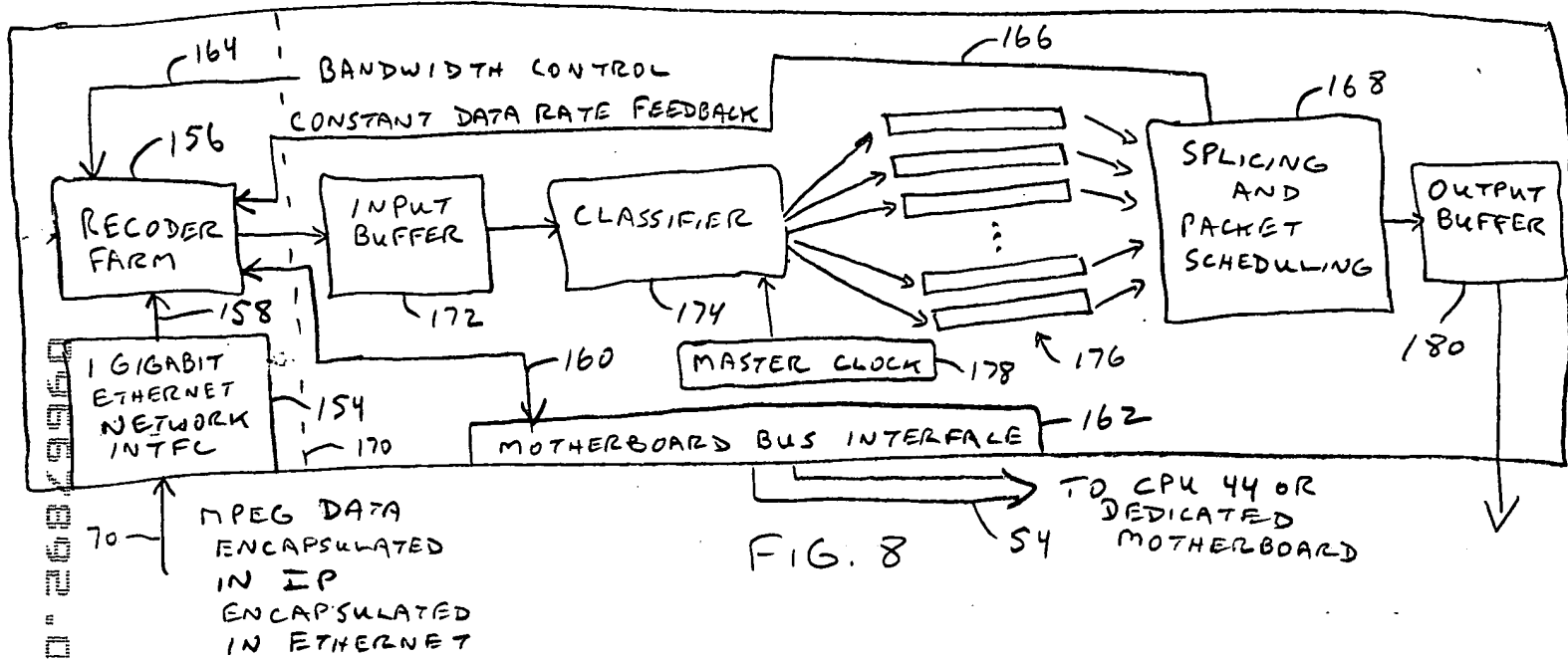
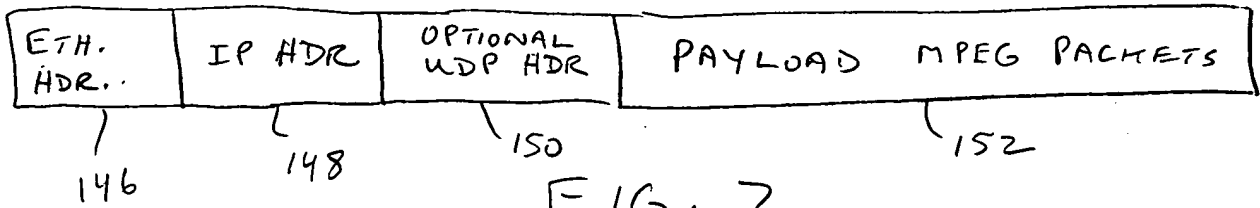


FIG. 5

IP DEWRAPPER PROCESS FOR DSL OR HFC ENVIRONMENTS

FIG. 6





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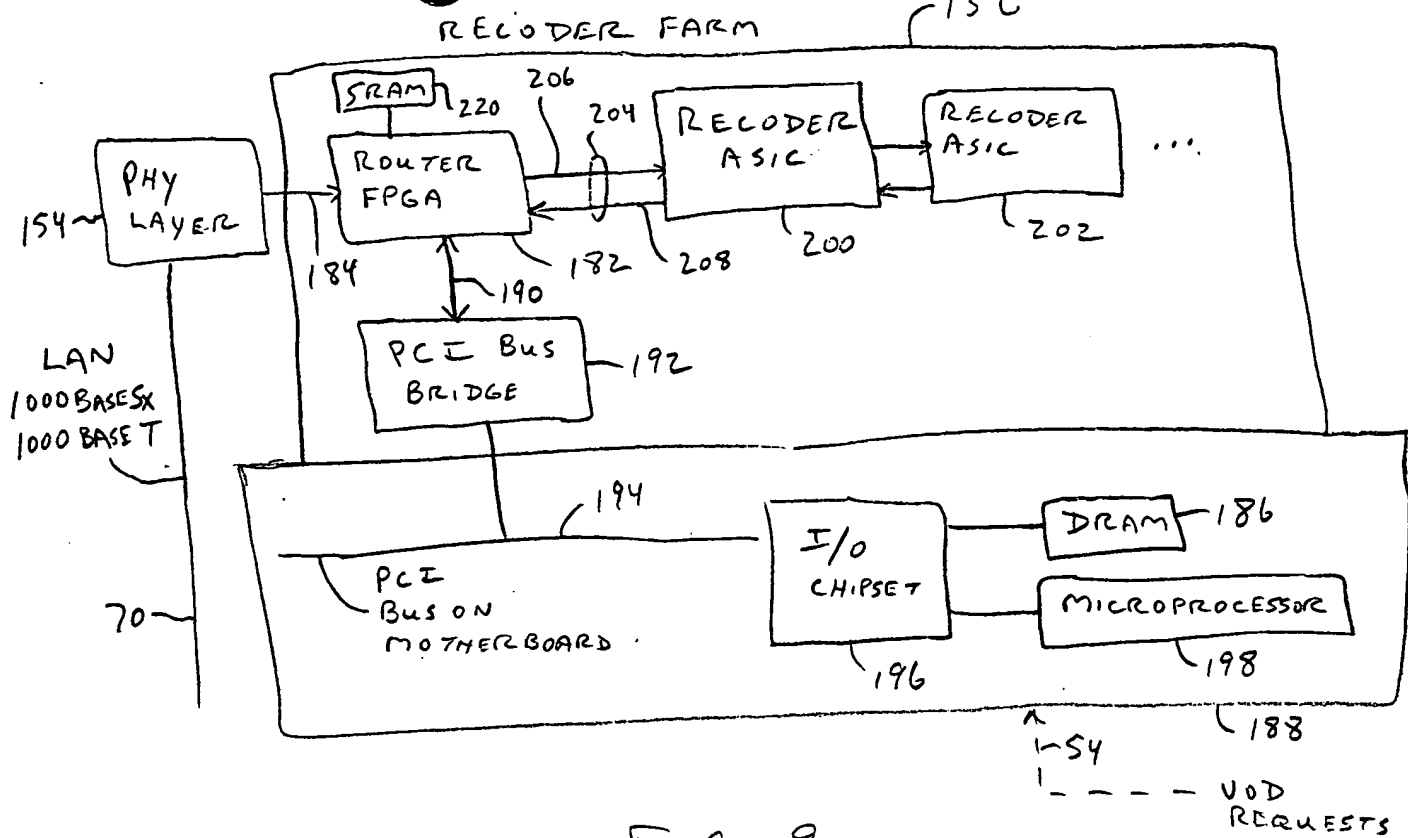


FIG. 9

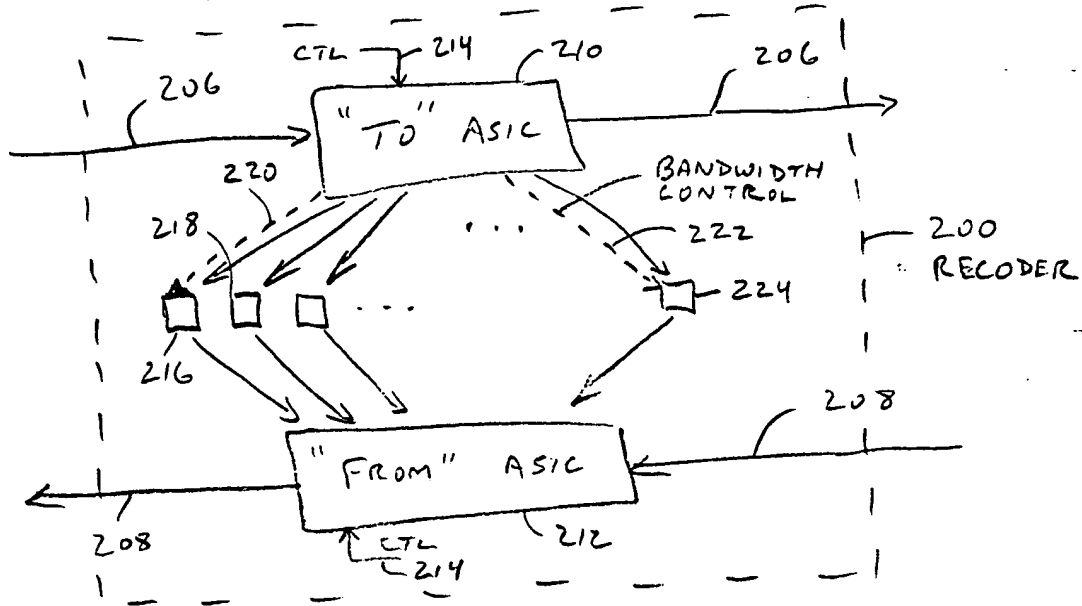


FIG. 10

002250-2684950

HEADEND ARCHITECTURE TO SEND DATA AND VOD AND/OR BROADCAST DATA TO CUSTOMERS VIA HFC

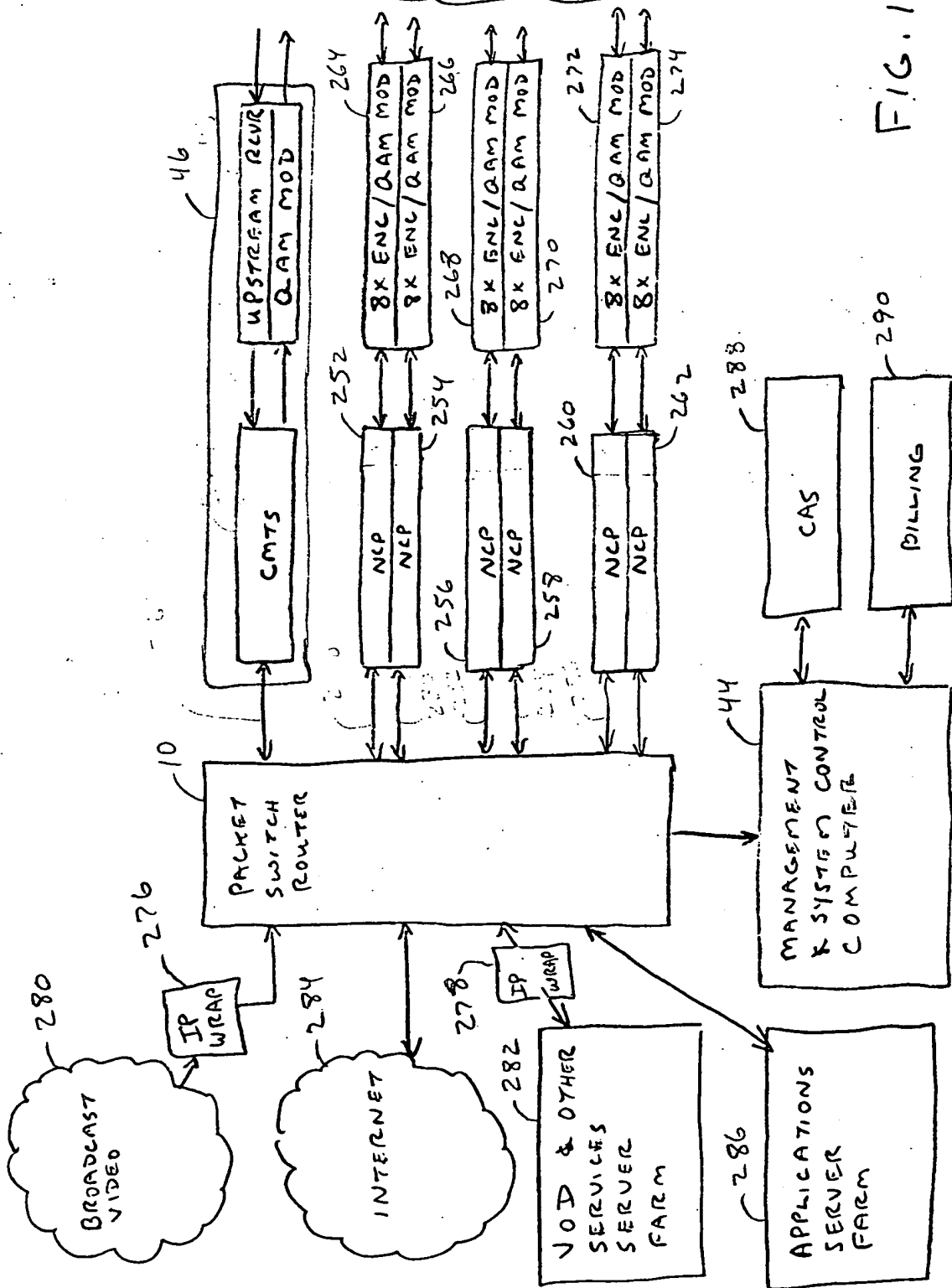


FIG. 11

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EMBODIMENT FOR TRANSMISSION OF DATA AND VIDEO PROGRAM DATA FROM HEADEND TO CUSTOMERS

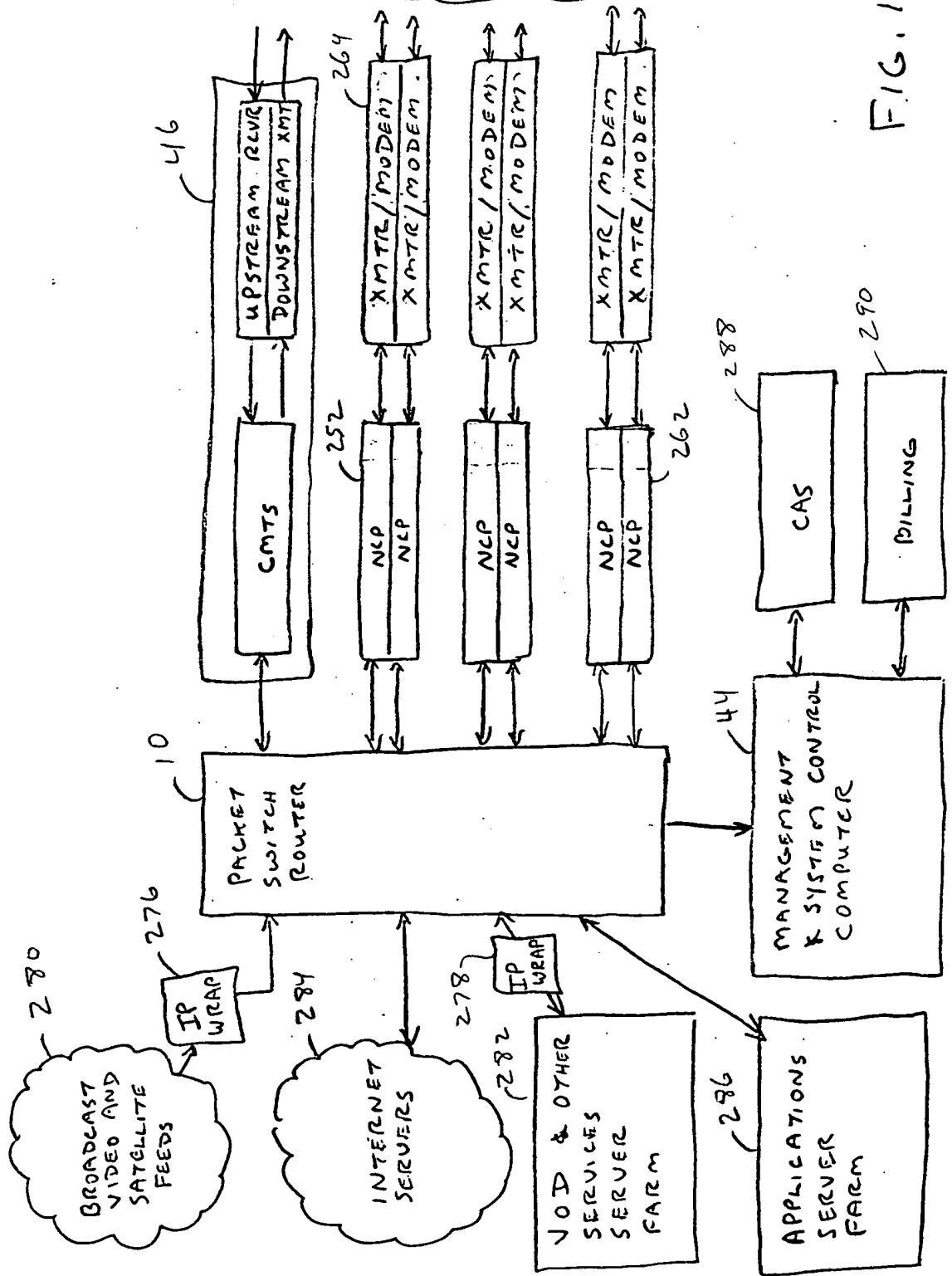


FIG. 12